
HA13557AFH

Combo (Spindle & VCM) Driver

HITACHI

ADE-207-234A (Z)

2nd. Edition

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Description

This COMBO Driver for HDD application consists of Sensorless Spindle Driver and BTL type VCM Driver.

Bipolar Process is applied and a “Soft Switching Circuit” for less commutation noise and a “Booster Circuit” for smaller Saturation Voltage of Output Transistor are also implemented.

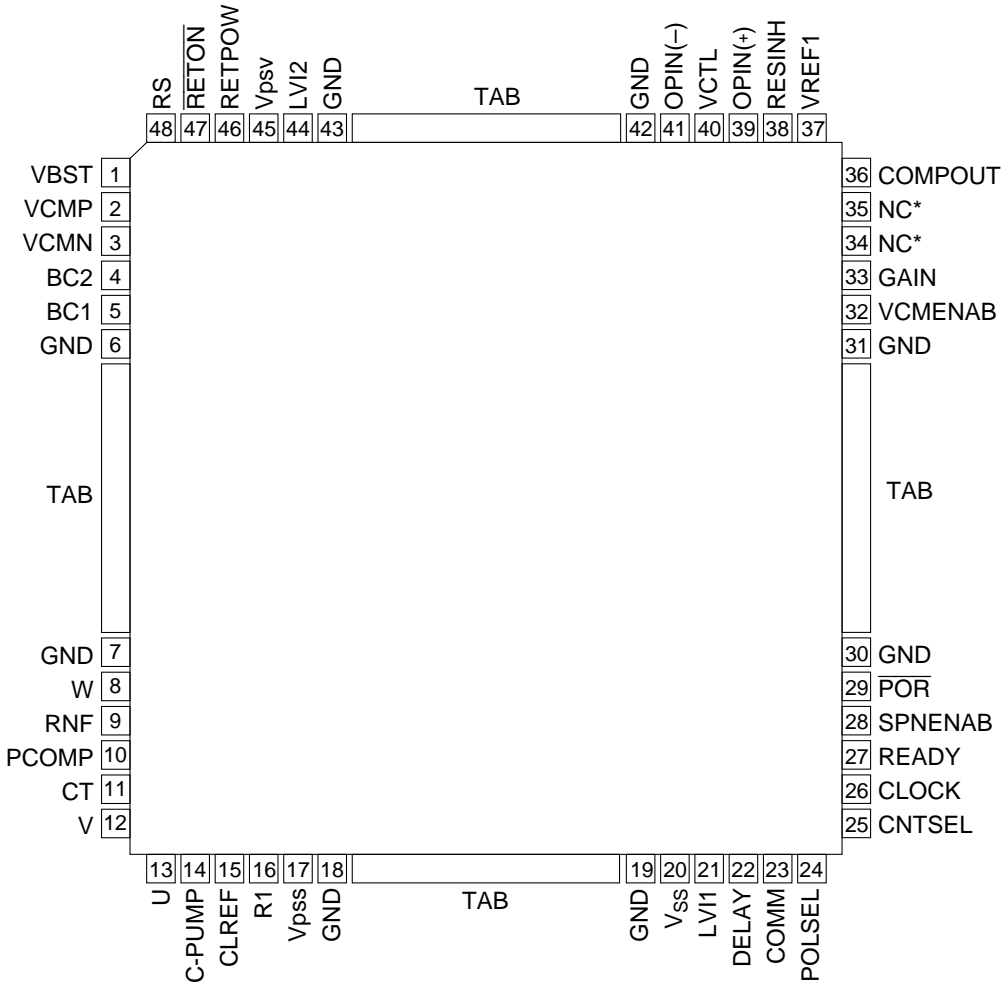
Features

- Soft Switching Driver
- Small Surface Mount Package: FP-48T (QFP48 Pin)
- Low thermal resistance: 30°C/W with 4 layer multi glass-epoxy board
- Low output saturation voltage
 - Spindle 1.44 V Typ (@1.8 A)
 - VCM 1.0 V Typ (@1.0 A)

Functions

- 2.2 A Max/3-phase motor driver
- 1.5 A Max BTL VCM Driver
- Auto retract
- Soft Switching Matrix
- Start up circuit
- Booster
- Speed Discriminator
- Internal Protector (OTSD, LVI)
- POR
- Power monitor

Pin Arrangement



*NC : No internal connection

Please note that there is no isolation check between pin 34 and pin 35 at the testing of this IC.

(Top View)

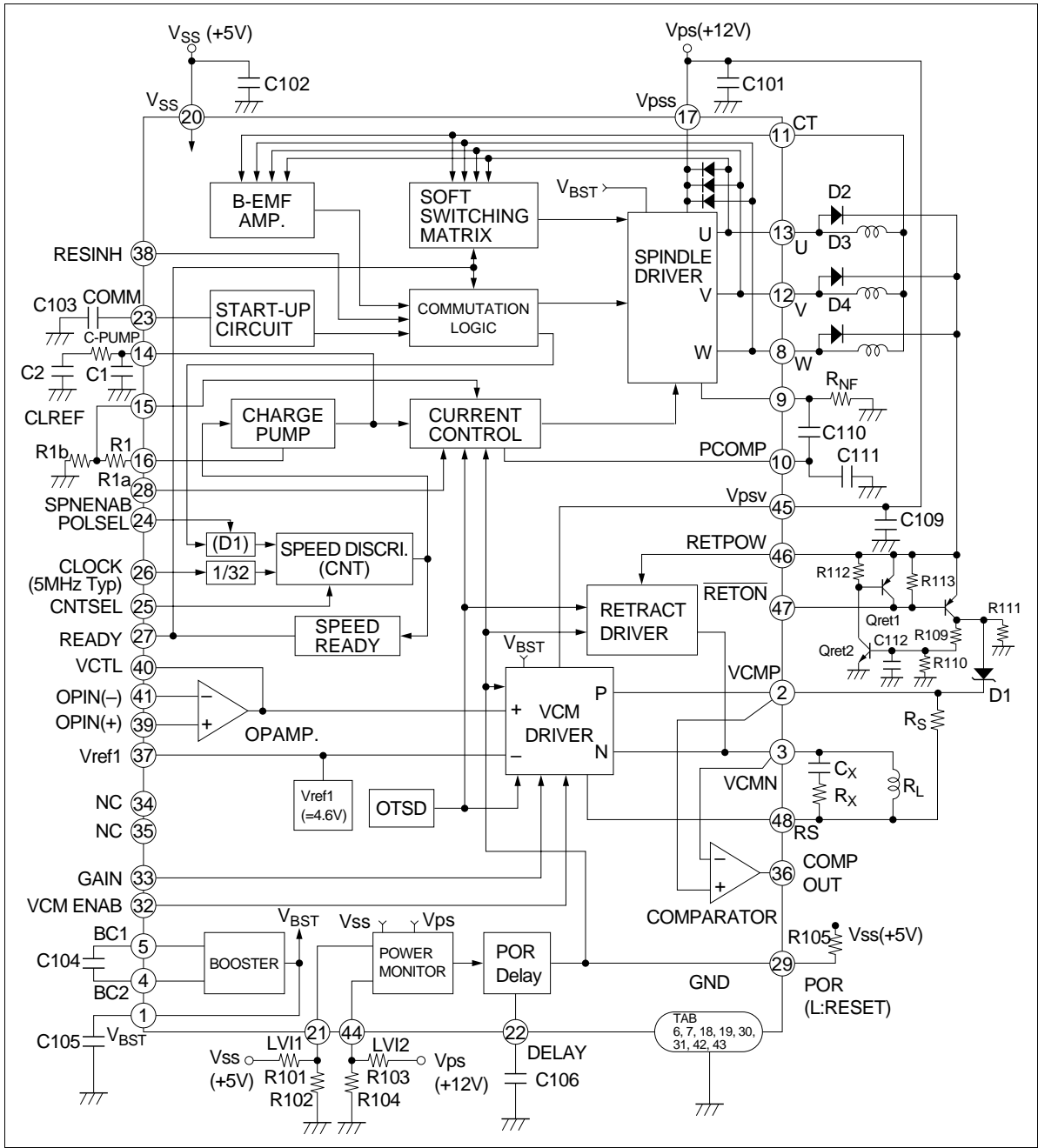
Pin Description

Pin Number	Pin Name	Function
1	VBST	Boosted voltage output to realize the low output saturation voltage
2	VCMP	Output terminal on VCM driver
3	VCMN	Output terminal on VCM driver
4	BC2	To be attached the external capacitor for booster circuitry
5	BC1	ditto
6, TAB, 7	GND	Ground pins
8	W	W phase output terminal on spindle motor driver
9	RNF	Sensing input for output current on spindle motor driver
10	PCOMP	To be attached the external capacitor for phase compensation of spindle motor driver
11	CT	To be attached the center tap of the spindle motor for B-EMF sensing
12	V	V phase output terminal on spindle motor driver
13	U	U phase output terminal on spindle motor driver
14	C-PUMP	To be attached the external integral constants for speed control of spindle motor
15	CLREF	Reference voltage input for current limiter of spindle motor driver
16	R1	To be attached the external resistor for setting up the oscillation frequency of start-up circuitry and the gain of speed control loop of spindle motor driver
17	Vpss	Power supply for spindle motor driver
18, TAB, 19	GND	Ground pins
20	V _{ss}	Power supply for small signal block
21	LVI1	Sensing input for power monitor circuitry
22	DELAY	To be attached the external capacitor to generate the delay time for power on reset signal
23	COMM	To be attached the external capacitor for setting up the oscillation frequency
24	POLSEL	To be selected the input status corresponding to the pole number of spindle motor
25	CNTSEL	To select the count Number of Speed Discriminator
26	CLOCK	Master clock input for this IC
27	READY	Output of speed lock detector for spindle motor
28	SPNENAB	To select the status of spindle motor driver
29	$\overline{\text{POR}}$	Output of power on reset signal for HDD system
30, TAB, 31	GND	Ground pins
32	VCMENAB	To select the status of VCM driver
33	GAIN	To select the Transfer conductance gm of VCM driver

Pin Description (cont)

Pin Number	Pin Name	Function
34	NC	No function
35	NC	No function
36	COMPOUT	Comparator output to detect the direction of output current on VCM driver
37	VREF1	Regulated voltage output to be used as reference of peripheral ICs
38	RESINH	Used for inhibiting the restart function of the spindle motor driver after power down
39	OPIN (+)	Non inverted input of OP.Amp. to be used for filtering the signal on PWMOUT
40	VCTL	OP.Amp. output, this signal is used as control signal for VCM driver output
41	OPIN (-)	Inverted input of OP.Amp. to be used for filtering the signal on PWMOUT
42, TAB, 43	GND	Ground pins
44	LVI2	Sensing input for power monitor circuitry
45	Vpsv	Power supply for VCM driver
46	RETPOW	Power supply for retract circuitry
47	RETON	To be attached the base terminal of external transistor for retracting
48	RS	Sensing input for output current on VCM driver

Block Diagram



Truth Table**Table 1 Truth Table (1)**

SPNENAB	Spindle Driver
H	ON
Open	Cut off
L	Braking

Table 2 Truth Table (2)

VCMENAB	VCM Driver
H	ON
L	Cut off

Table 3 Truth Table (3)

OTSD	Spindle Driver	VCM Driver	Retract Driver	$\overline{\text{POR}}$
not Active	See table 1	See table 2	Cut off	X
Active	Cut off	Cut off	ON	L

Table 4 Truth Table (4)

POLSEL	(D1)	Comment
H	—	Test Mode
Open	1/12	for 8 poles motor
L	1/18	for 12 poles motor

Table 5 Truth Table (5)

CNTSEL	CNT	Rotation Speed (at CLOCK = 5 MHz)
H	2605	3,600 rpm
Open	2084	4,500 rpm
L	1736	5,400 rpm

Table 6 Truth Table (6)

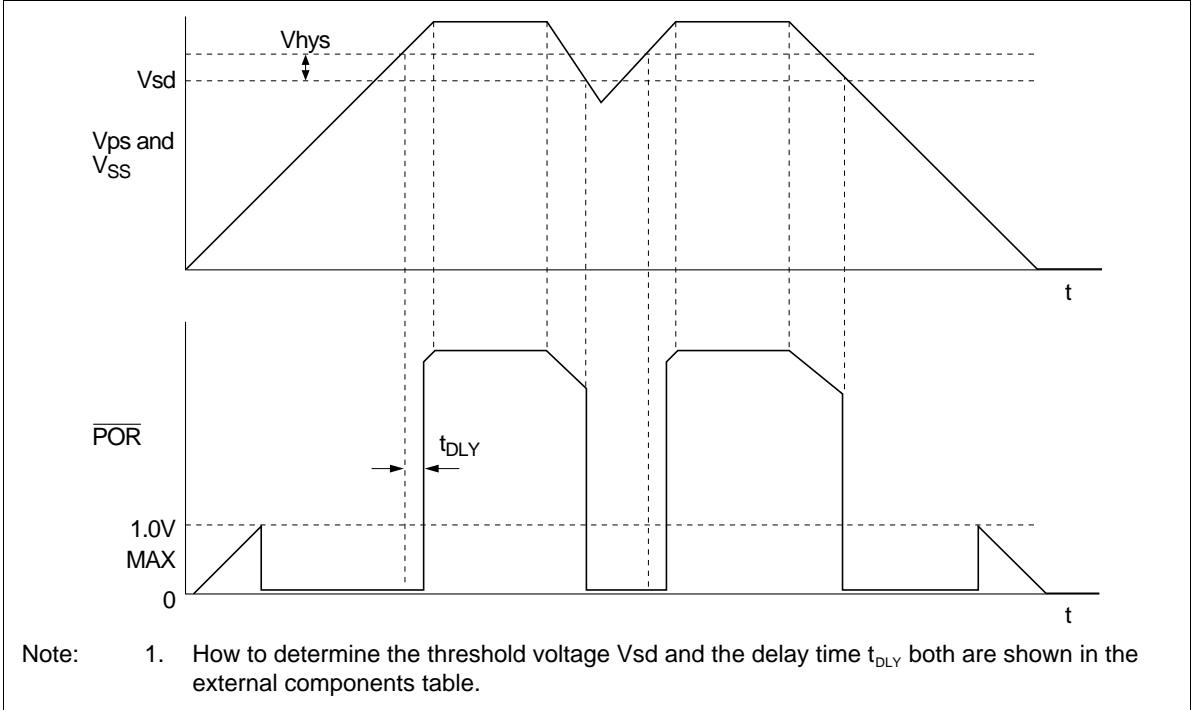
RESINH	Spindle Driver
H	Inhibiting the restart after power down
L	Not inhibiting the restart after power down

Table 7 Truth Table (7)

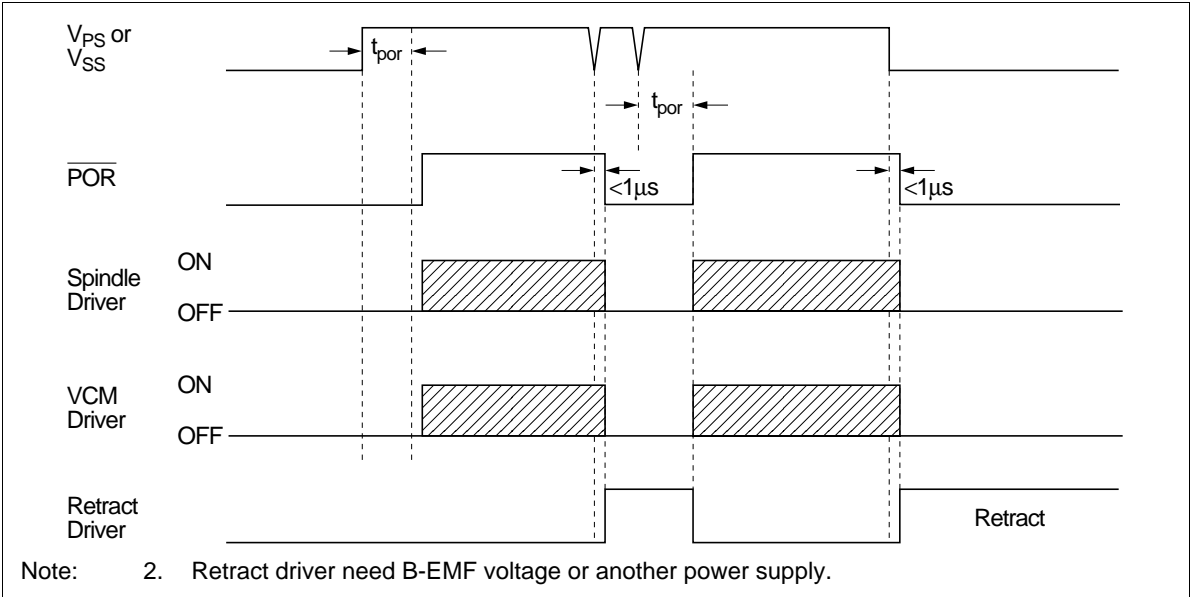
GAIN	VCM Driver
H	High Gain Mode
L	Low Gain Mode

Timing Chart

1. Power on reset (1)

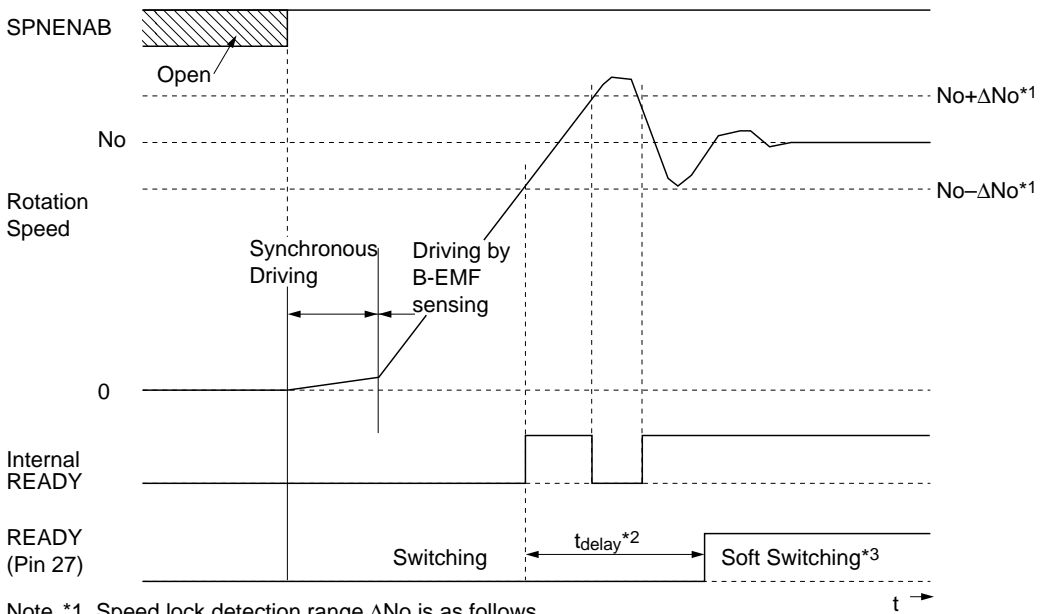


2. Power on reset (2)



3. Motor start-up sequence

(a) Timing chart of start-up sequence



Note *1. Speed lock detection range ΔNo is as follows.

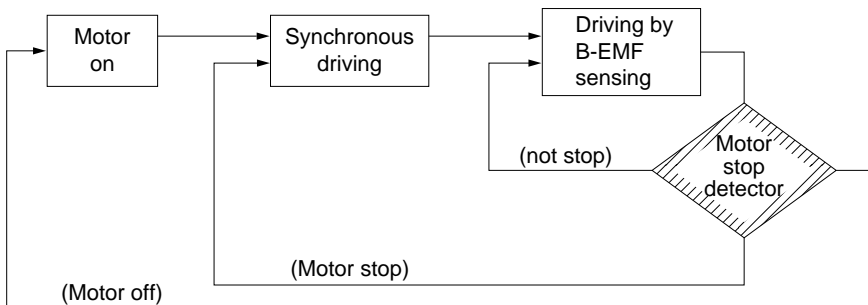
$$\begin{aligned} \Delta No &= 1.2\% \text{ when CNTSEL}=\text{H} \\ &= 1.5\% \text{ when CNTSEL}=\text{Open} \\ &= 1.8\% \text{ when CNTSEL}=\text{L} \end{aligned}$$

*2. READY output goes to High, if the rotation speed error keeps to be less than ΔNo longer time than t_{delay} .

$$t_{\text{delay}} = \frac{250 \cdot 10^7}{\text{fclk [Hz]}} \text{ [ms]}$$

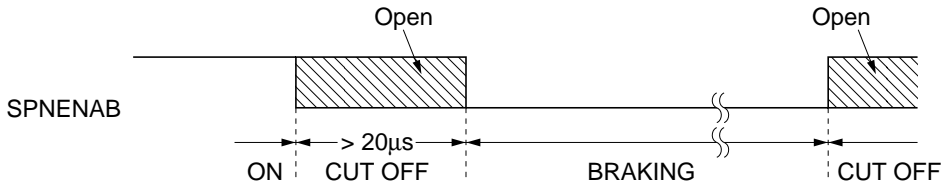
*3. The turning point of driving mode from switching synchronize to the turning point of READY output from Low to High.

(b) Retry circuitry for misstart-up



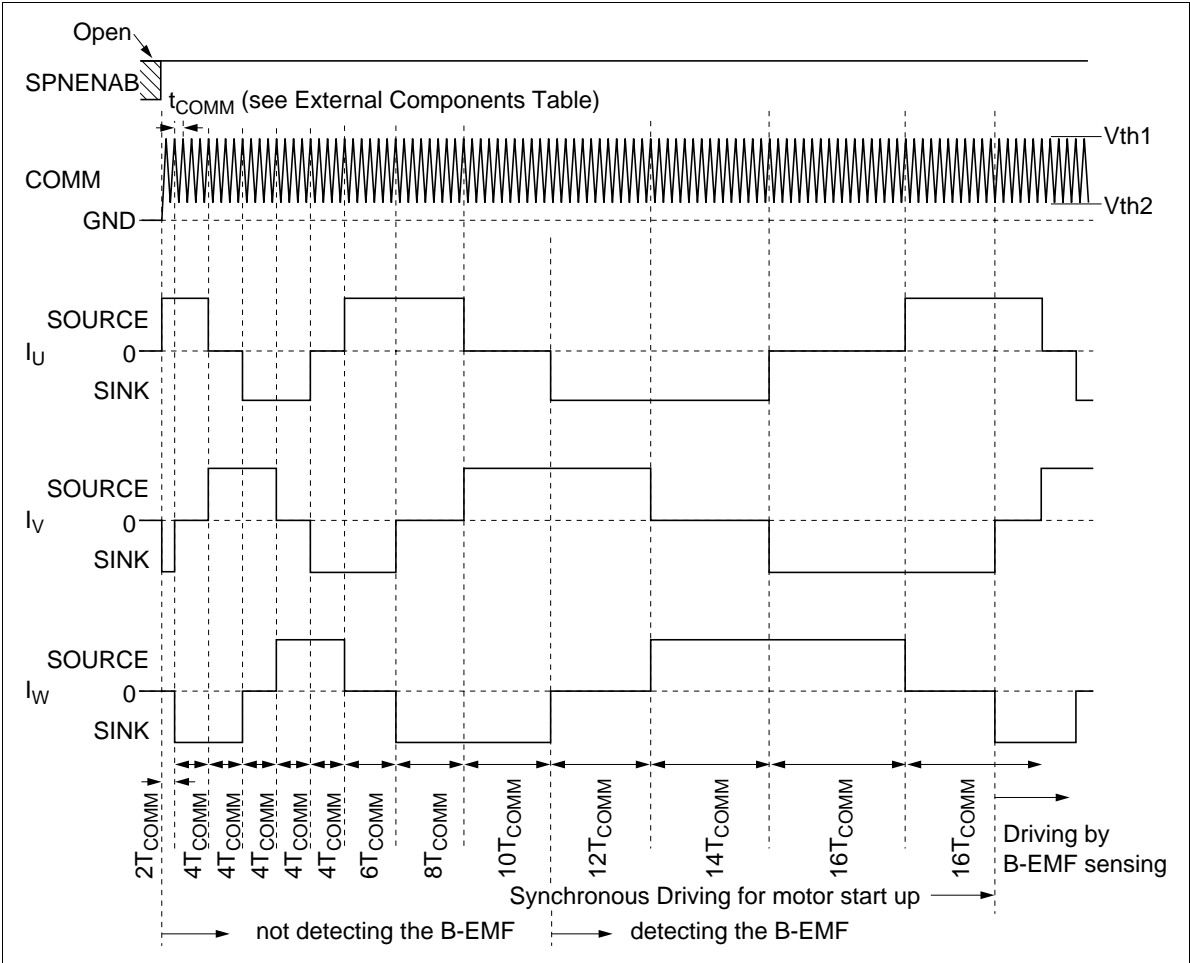
The HA13557FH has the motor stop detector as shown hatching block. This function is monitoring the situation of the motor while the motor is running by B-EMF sensing. If the motor will be caused a misstarting up, the motor will be automatically restarted within 200 ms after the motor stopped. This function increase the reliability for the motor starting up.

4. Braking & Shut down the Spindle Driver

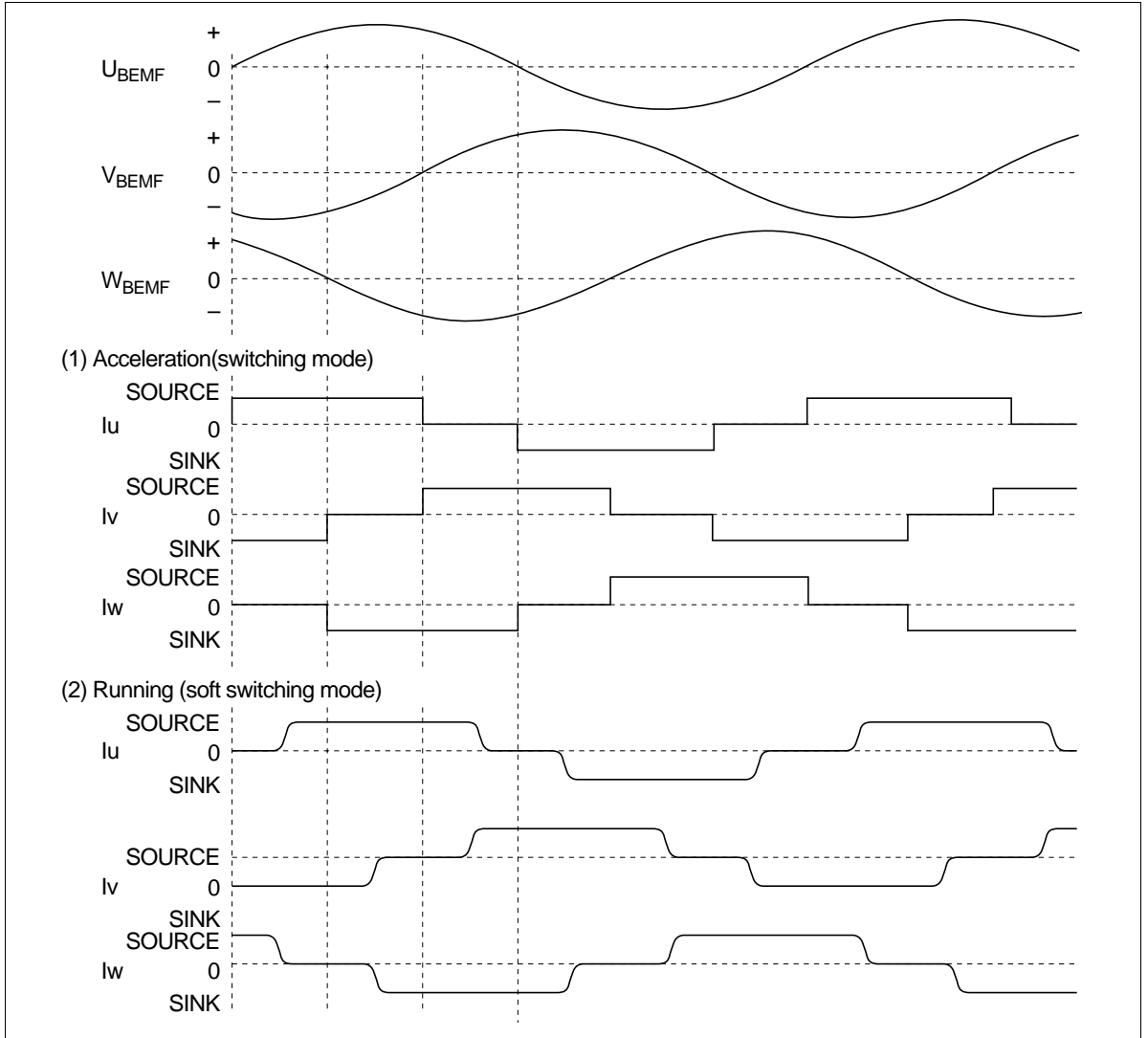


Note: The SPENAB should be selected the open state after braking to reduce the supply current from V_{ps} and V_{ss} .

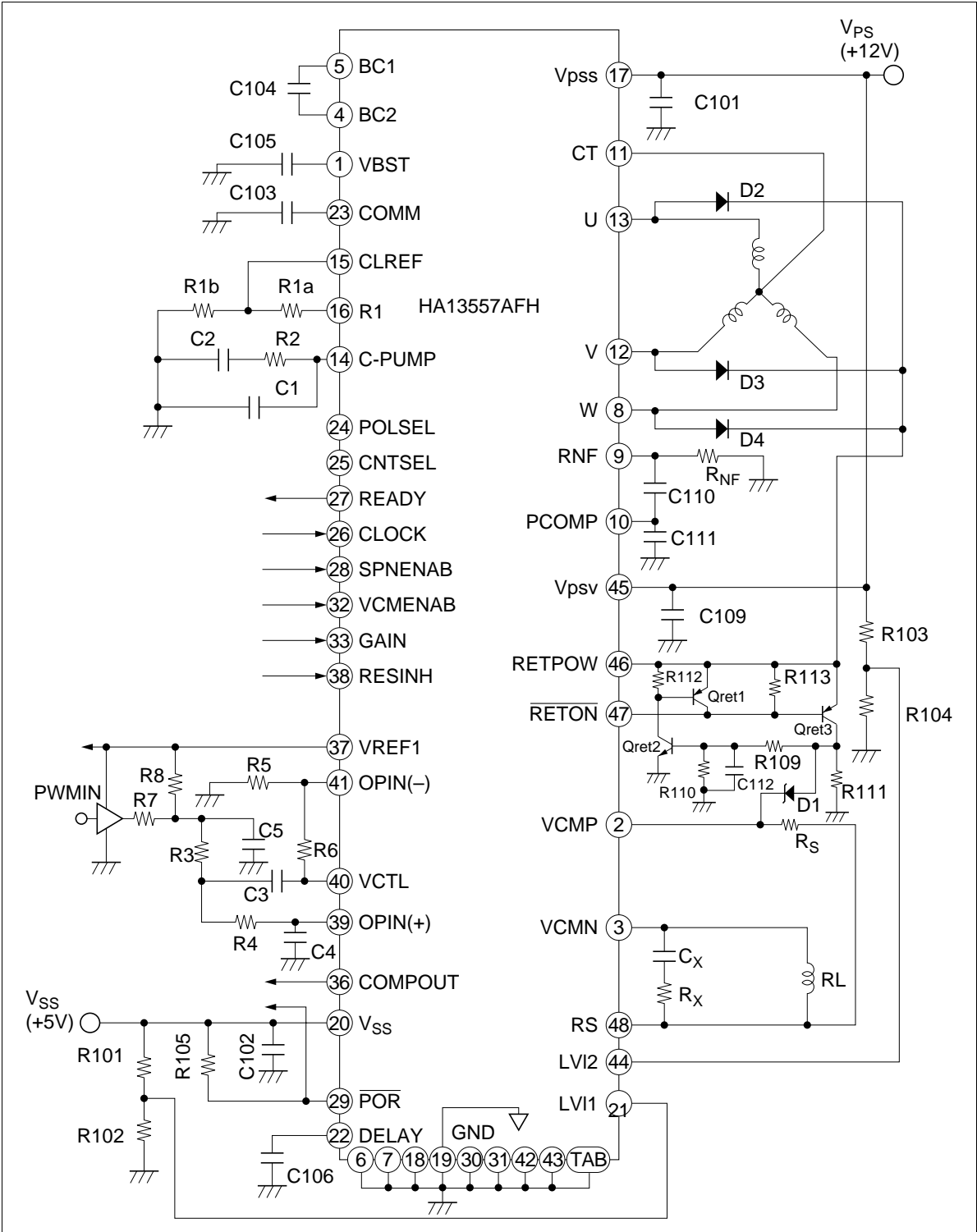
5. Start-up of the Spindle motor



6. Acceleration and Running the spindle motor



Application



External Components

Parts No.	Recommended Value	Purpose	Note
R1a	$(R1a + R1b) \geq 10 \text{ k}\Omega$	V/I converter	1, 4, 6
R1b	$(R1a + R1b) \geq 10 \text{ k}\Omega$		
R2	—	Integral constant	3
R3 to R8	—	PWM filter	9
R101, R102	—	Setting of LVI1 voltage	7
R103, R104	—	Setting of LVI2 voltage	7
R105	5.6 k Ω	Pull up	
R109, R110	$(R109 + R110) \geq 10 \text{ k}\Omega$	Retout voltage adjust	
R111, R112, R113	—	Retract Driver	
RS	1.0 Ω	Current sensing for VCM Driver	10
Rnf	—	Current sensing for Spindle Driver	1
R _x	—	Reduction for gain peaking	11
C1, C2	—	Integral constant	3
C3 to C6	—	PWM filter	9
C _x	—	Reduction for gain peaking	11
C101	$\geq 0.1 \mu\text{F}$	Power supply by passing	
C102	$\geq 0.1 \mu\text{F}$	Power supply by passing	
C103	—	Oscillation for start-up	6
C104	0.22 μF	for booster	
C105	2.2 μF	for booster	
C106	$\leq 0.33 \mu\text{F}$	Delay for POR	8
C109	$\geq 0.1 \mu\text{F}$	Power supply by passing	
C110, C111	0.22 μF	Phase compensation	
C112	—	Phase compensation for Retract	
Qret1, Qret2, Qret3	—	Retract Driver	12
D1	TBD	Prevent of counter current	
D2, D3, D4	Si • Diode	for rectification	

Notes: 1. Output maximum current on spindle motor driver I_{spnmax} is determined by following equation.

$$I_{spnmax} = \frac{R1b}{R1a + R1b} \cdot \frac{V_{R1}}{R_{NF}} \quad [A] \quad (1)$$

where, V_{R1} : Reference Voltage on Pin 16 [V] (= 1.17)

2. Input clock frequency f_{clk} on pin 26 is determined by following equation.

$$f_{clk} = \frac{4}{5} \cdot N_O \cdot P \cdot D1 \cdot (CNT - 0.5) \quad [Hz] \quad (2)$$

where, N_O : Standard rotation speed [rpm]

P : Number of pole

$D1$: Dividing ratio on divider 1

$D1 = 1/12$ (when Pin 24 = Open) for 8 pole motor

$= 1/18$ (when Pin 24 = Low) for 12 pole motor

CNT : Count number on speed discriminator

$CNT = 2605$ (when Pin 25 = High)

$= 2084$ (when Pin 25 = Open)

$= 1736$ (when Pin 25 = Low)

3. Integral constants $R2$, $C1$ and $C2$ can be designed as follows.

$$\omega_O = \frac{1}{10} \cdot 2 \cdot \pi \cdot \frac{N_O}{60} \quad [rad/s] \quad (3)$$

$$R2 = \frac{1}{9.55} \cdot \frac{R_{nf} \cdot J \cdot \omega_O \cdot N_O \cdot (R1a + R1b)}{V_{R1} \cdot K_T \cdot G_{ctl}} \quad [\Omega] \quad (4)$$

$$C1 = \frac{1}{\sqrt{10} \cdot \omega_O \cdot R2} \quad [F] \quad (5)$$

$$C2 = 10 \cdot C1 \quad [F] \quad (6)$$

where, J : Moment of inertia [$kg \cdot cm \cdot s^2$]

K_T : Torque constant [$kg \cdot cm/A$]

G_{ctl} : Current control amp gain from pin 14 to pin 9 (= 0.794)

4. It is notice that rotation speed error N_{error} is caused by leak current I_{cer2} on pin 14 and this error depend on $R1a$ and $R1b$ as following equation.

$$N_{error} = I_{cer2} \cdot \frac{(R1a + R1b)}{V_{R1}} \cdot 100 \quad [\%] \quad (7)$$

where, I_{cer2} : leak current on pin 14 [A]

5. Oscillation period t_{COMM} on pin 23 which period determine the start up characteristics, is should be chosen as following equation.

$$t_{COMM} = \frac{1}{8} \cdot \sqrt{\frac{J}{P \cdot K_T \cdot I_{spnmax}}} \quad \text{to} \quad \frac{1}{4} \cdot \sqrt{\frac{J}{P \cdot K_T \cdot I_{spnmax}}} \quad [s] \quad (8)$$

6. The capacitor C103 on pin 23 can be determined by t_{COMM} and following equation.

$$C103 = \frac{1}{4} \cdot \frac{VR1}{R1a + R1b} \cdot \frac{t_{COMM}}{V_{thH} - V_{thL}} \quad [F] \quad (9)$$

where, V_{thH} : Threshold voltage on start up circuit [V] (= 2.0)

V_{thL} : Threshold voltage on start up circuit [V] (= 0.5)

7. LVI operating voltage Vsd1, Vsd2 and its hysteresis voltage Vhys1, Vhys2 can be determined by following equations.

for V_{SS}

$$Vsd1 = \left(1 + \frac{R101}{R102}\right) \cdot Vth4 \quad [V] \quad (10)$$

$$Vhys1 = \left(1 + \frac{R101}{R102}\right) \cdot Vhyspm \quad [V] \quad (11)$$

for V_{ps}

$$Vsd2 = \left(1 + \frac{R103}{R104}\right) \cdot Vth3 \quad [V] \quad (12)$$

$$Vhys2 = \left(1 + \frac{R103}{R104}\right) \cdot Vhyspm \quad [V] \quad (13)$$

where, $Vth3, Vth4$: Threshold voltage on pin 21 and pin 44 [V] (= 1.39)

$Vhyspm$: Hysteresis voltage on pin 21 and pin 44 [mV] (= 40)

Shut down voltage Vsd1, Vsd2 can be designed by the following range.

$Vsd1 \geq 4.25$ [V], $Vsd2 \geq 10$ [V]

8. The delay time t_{DLY} of \overline{POR} for power on reset is determined as follows.

$$t_{DLY} = \frac{C106 \cdot Vth5}{I_{CH3}} \quad [s] \quad (14)$$

where, $Vth5$: Threshold voltage on pin 22 [V] (= 1.4)

I_{CH3} : Charge current on pin 22 [μ A] (= 6)

9. The differential voltage ($V_{ctl} - V_{REF1}$) using for control of VCM driver depend on PWM DAC input PWMIN as follows.

$$V_{ctl} - V_{REF1} = 2 \cdot V_{REF1} \cdot \frac{D_{PWM} - 50}{100} \cdot \frac{R6}{R5} \cdot H_{FLT(S)} \quad (15)$$

where, D_{PWM} : Duty cycle on PWMIN [%]

$H_{FLT(S)}$: Normalized transfer function from PWMIN to pin 40 (V_{ctl}) as shown in equation (17)

To be satisfied with above equation (15), it is notice that the ratio of R6 to R7 must be chosen as shown below.

$$\frac{R8}{R7} = 2 \cdot \frac{R6}{R5} \cdot \frac{1}{1 - \frac{R6}{R5}} \quad (16)$$

$$H_{FLT}(s) = \frac{1}{1 + s \left[C5 \cdot R// - C3 \cdot (R// + R3) \cdot \frac{R6}{R5} + C4 \cdot (R// + R3 + R4) \right] + s^2 \left[C5 \cdot C4 \cdot R// \cdot (R3 + R4) - C5 \cdot C3 \cdot R// \cdot R3 \cdot \frac{R6}{R5} + C3 \cdot C4 \cdot R4 \cdot (R// + R3) \right] + s^3 \cdot C3 \cdot C4 \cdot C5 \cdot R// \cdot R3 \cdot R4} \quad (17)$$

where, $R// = \frac{R7 \cdot R8}{R7 + R8}$ (18)

If you choose the $R// \ll R3$, then equation (17) can be simplified as following equation.

$$H_{FLT}(s) = \frac{1}{1 + \frac{s}{\omega_0}} \cdot \frac{1}{1 + 2 \cdot \zeta \cdot \left(\frac{s}{\omega_n}\right) + \left(\frac{s}{\omega_n}\right)^2} \quad (19)$$

where,

$$\omega_0 = \frac{1}{C5 \cdot R//} \quad (20)$$

$$\omega_n = \frac{1}{\sqrt{C3 \cdot C4 \cdot R3 \cdot R4}} \quad (21)$$

$$\zeta = \frac{C4 \cdot (R3 + R4) - C3 \cdot R3 \cdot \frac{R6}{R5}}{2 \cdot \sqrt{C3 \cdot C4 \cdot R3 \cdot R4}} \quad (22)$$

10. The relationship between the output current I_{vcm} and the input voltage ($V_{ctl} - V_{REF1}$) on VCM driver is as follows.

$$I_{vcm}(s) = \left(V_{ctl} - V_{REF1} \right) \cdot K_{vcm} \cdot \frac{1}{R_s} \cdot H_{vcm}(s) \quad (23)$$

where, V_{ctl} : Input control voltage for VCM driver on pin 40 [V]

V_{REF1} : Reference voltage on pin 37 [V] (= 4.6)

K_{vcm} : DC gain of VCM driver
 (= 1.74 for High gain mode)
 (= 0.44 for Low gain mode)

$H_{vcm}(s)$: Transfer function of VCM driver as shown following equation

$$H_{vcm}(s) = \frac{1}{1 + 2 \cdot \zeta_{VCM} \cdot \left(\frac{s}{\omega_{VCM}}\right) + \left(\frac{s}{\omega_{VCM}}\right)^2} \quad (24)$$

where,

$$\omega_{VCM} = \sqrt{\omega_p \cdot \frac{R_s}{L_m}} \quad (25)$$

$$\zeta_{VCM} = \frac{1}{2} \cdot \left(1 + \frac{R_L}{R_s} \right) \cdot \sqrt{\frac{1}{\omega_P} \cdot \frac{R_s}{L_m}} \tag{26}$$

where, ω_P : Bandwidth of internal power amplifiers for VCM driver [rad/s]
 (= $3 \cdot \pi \cdot 10^6$)

L_m : Inductance of the VCM coil [H]

R_L : Resistance of the VCM coil [Ω]

and from above equations the -3 dB bandwidth f_{VCMC} of VCM driver is as following equation.

$$f_{VCMC} = \frac{\omega_{VCM}}{2 \cdot \pi} \cdot \sqrt{\left[1 - 2 \cdot \zeta_{VCM}^2 \right] + \sqrt{\left[2 \cdot \zeta_{VCM}^2 - 1 \right]^2 + 1}} \tag{27}$$

11. The frequency response of VCM driver maybe have a gain peaking because of the resonance of the motor coil impedance. If you want to tune up for this characteristics, you can reduce the peaking by additional snubber circuit R_x and C_x as follows.

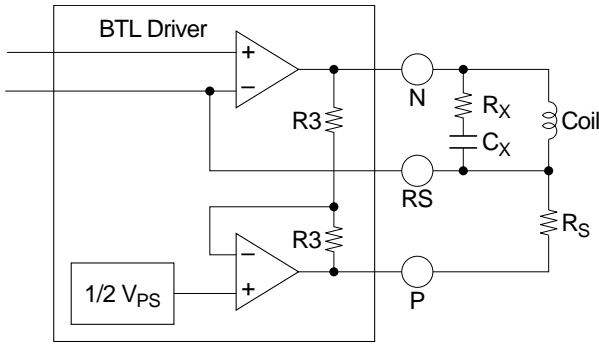
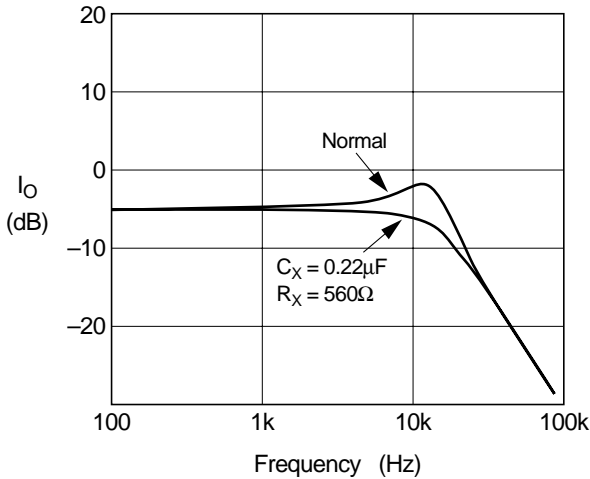


Figure 1 VCM Driver Block Diagram



(for example) $R_L = 14.7 \Omega$, $R_s = 1 \Omega$, $L = 1.7 \text{ mH}$, Gain = L

12. The Qret3 collector voltage V_{ret} is determined by

$$V_{ret} = V_{RT} \left(\frac{R_{109}}{R_{110}} + 1 \right) \quad (V_{retpow} \geq V_{RT} \left(\frac{R_{109}}{R_{110}} + 1 \right))$$

$$I_{ret} \doteq \frac{V_{ret} - V_F(D1) - V_{sat_{VL}}}{R_L + R_s} \quad (28)$$

where, V_{retpow} : Applied voltage on pin 46 [V]
 V_{RT} : Reference voltage of Retract (toward voltage of Qret2) [V]
 $V_F(D1)$: Forward voltage of D1 [V]
 $V_{sat_{VL}}$: Saturation voltage on pin 3 at retracting [V]
 (See electrical characteristics)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Notes
Power supply voltage	Vps	+15	V	1
Signal supply voltage	V _{SS}	+7	V	2
Input voltage	V _{IN}	V _{SS}	V	3
Output current-Spindle	I _{ospn} (Peak)	2.2	A	
	I _{ospn} (DC)	1.8	A	
Output current-VCM	I _{ovcm} (Peak)	1.5	A	
	I _{ovcm} (DC)	1.0	A	
Power dissipation	P _T	5	W	4
Junction temperature	T _J	+150	°C	5, 6
Storage temperature	T _{stg}	-55 to +125	°C	

Notes: 1. Operating voltage range is 10.2 V to 13.8 V.

2. Operating voltage range is 4.25 V to 5.75 V.

3. Applied to Pin 24, 25, 26, 28, 32, 33 and pin 38

4. Operating junction temperature range is T_{jop} = 0°C to +125°C.

5. ASO of upper and lower power transistor are shown below.

Operating locus must be within the ASO.

6. The OTSD (Over Temperature Shut Down) function is built in this IC to avoid same damages by over heat of this chip. However, please note that if the junction temperature of this IC becomes higher than the operating maximum junction temperature (T_{jopmax} = 125°C), the reliability of this IC often goes down.

7. Thermal resistance: $\theta_{j-a} \leq 30^\circ\text{C/W}$ with 4 layer multi glass-epoxy board

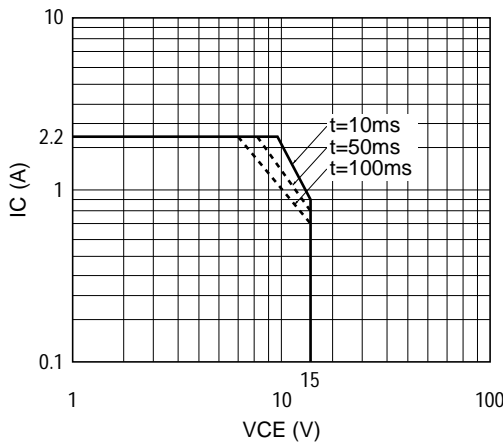


Figure 2 ASO of Output Stages (Spindle)

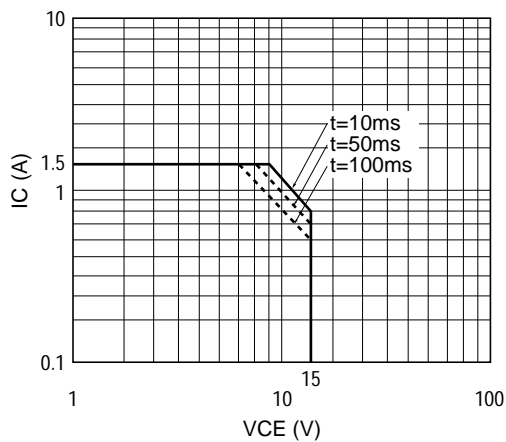


Figure 3 ASO of Output Stages (VCM)

Electrical Characteristics (Ta = 25°C, Vps = 12 V, Vss = 5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Supply current	for V _{SS}	I _{SS0}	—	5.8	7.0	mA	SPNENAB = Open VCMENAB = L	20	
		I _{SS1}	—	21	27	mA	SPNENAB = H VCMENAB = H	20	
	for Vps	I _{ps0}	—	1.7	2.2	mA	SPNENAB = Open VCMENAB = L	17, 45	
		I _{ps1}	—	19	24	mA	SPNENAB = H VCMENAB = H	17, 45	
Logic input 1 (GAIN) (RESINH)	Input low voltage	V _{IL1}	—	—	0.8	V		33, 38	
	Input high voltage	V _{IH1}	2.0	—	—	V			
	Input low current	I _{IL1}	—	—	±10	μA	Input = GND		
	Input high current	I _{IH1}	—	—	±10	μA	Input = 5.0 V		
Logic input 2 (CLOCK)	Input low voltage	V _{IL2}	—	—	0.8	V		26	
	Input high voltage	V _{IH2}	3.5	—	—	V			
	Input low current	I _{IL2}	—	-180	-260	μA	Input = GND		
	Input high current	I _{IH2}	—	230	330	μA	Input = 5.0 V		
Logic input 3 (VCMENAB)	Input low voltage	V _{IL3}	—	—	0.8	V		32	
	Input high voltage	V _{IH3}	2.0	—	—	V			
	Input low current	I _{IL3}	—	—	±10	μA	Input = GND		
	Input high current	I _{IH3}	—	—	330	μA	Input = 5.0 V		
Logic input 4 (SPNENB)	Input low voltage	V _{IL4}	—	—	1.0	V		28	
	Input middle voltage	V _{IM4}	2.0	—	3.1	V			
	Input high voltage	V _{IH4}	3.9	—	—	V			

Electrical Characteristics (Ta = 25°C, Vps = 12 V, Vss = 5 V) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Logic input 4 (SPNENB)	Input low current	I_{IL4}	-75	-105	-150	μA	Input = GND	28
	Input high current	I_{IH4}	75	105	150	μA	Input = 5.0V	
	Input dead current	I_{DEAD}	± 10	—	—	μA		
Logic input 5 (POLSEL) (CONTSEL)	Input low voltage	V_{IL5}	—	—	1.0	V		24, 25
	Input middle voltage	V_{IM5}	2.0	—	3.1	V		
	Input high voltage	V_{IH5}	3.9	—	—	V		
	Input low current	I_{IL5}	-38	-53	-75	μA	Input = GND	
	Input high current	I_{IH5}	38	53	75	μA	Input = 5.0V	
Spindle driver	Total saturation voltage	V_{satspn}	—	1.44	2.0	V	$I_{spn} = 1.8\text{A}$	8, 12, 13
			—	—	0.75	V	$I_{spn} = 0.6\text{A}$	
	Saturation at braking	V_{break}	—	—	0.7	V	$I_{break} = 0.6\text{A}$	
	Leak current	I_{cer1}	—	—	± 2.0	mA	SPNENAB=Open	
	Current limiter reference voltage	V_{OCL}	430	480	530	mV	$V_{CLREF} = 500\text{mV}$ $R_{NF} = 1.0\Omega$	9
	Control amp gain	G_{ctl}	—	-2	± 2	dB	$R_{NF} = 1.0\Omega$	9, 14
	Clamp diode forward voltage	V_{df}	1.6	1.9	2.2	V	$I_{df} = 0.5\text{A}$	8, 12, 13
B-EMF amp.	Input sensitivity	V_{min}	60	90	125	mVp-p		8, 12, 13
Charge pump	Reference voltage	V_{R1}	1.06	1.17	1.28	V	$R_{1a} + R_{1b} = 24\text{k}\Omega$	14, 16
	Charge current	I_{CH1}	40	45	50	μA	$C - \text{PUMP} = 1.0\text{V}$	
	Discharge current	I_{DIS1}	-40	-45	-50	μA		
	Leak current	I_{cer2}	—	—	± 50	nA		

Electrical Characteristics (Ta = 25°C, Vps = 12 V, Vss = 5 V) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Speed discri	Operating frequency	fclk	—	—	8.0	MHz	26	
Start up circuit	Threshold voltage	Vth _H	1.6	1.8	2.0	V		16, 23
		Vth _L	0.3	0.5	0.7	V		
	Charge current	I _{CH2}	21	23	26	μA	R1a + R1b = 24 kΩ	
	Discharge current	I _{DIS2}	-19	-22	-25	μA	COMM = 1 V	
READY	Output high voltage	Vohr	V _{SS} - 0.4	—	V _{SS}	V	I _O = -1 mA	27
	Output low voltage	Volr	—	—	0.4	V	I _O = 1 mA	
VCM driver	Total saturation voltage	Vsatvcm	—	1.0	1.38	V	Ivcm = 1.0 A	2, 3
			—	0.5	0.69	V	Ivcm = 0.5 A	
	Output leak current	I _{cer3}	—	—	±2.0	mA	Vce = 15 V	
	Total output offset voltage	Voff(H)	—	—	±20	mV	V _{CTL} = OP (-) V _{REF} = OP (+)	2, 48
		Voff(L)	—	—	±10	mV		
	Output quiescent voltage	Vqvcm	5.6	6.0	6.4	V	R _L = 14 Ω, R _S = 1.0 Ω	2, 3
	Total gain bandwidth	B	—	26	—	kHz	R _S = 1.0 Ω, R _L = 28 Ω	2, 3
—			50	—	kHz	R _S = 1.0 Ω, R _L = 14 Ω		
Transfer gain	gm (H)	—	1.74	±5%	A/V	Higain-mode R _S = 1.0 Ω, R _L = 14 Ω	2, 34, 48	
	gm (L)	—	0.44	±5%	A/V	Logain-mode R _S = 1.0 Ω, R _L = 14 Ω		

Electrical Characteristics (Ta = 25°C, Vps = 12 V, Vss = 5 V) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Retract driver	Retpow voltage	Vretpow	0.8	—	—	V	Ireton = 0.1 mA	46
	Retout sink current	Ireton	5	8	—	mA	Vretpow = 4.0 V	
	Output leak current	Icer4	—	—	±10	μA	Vreton = 15 V, Vretpow = 15 V	37
	Low side saturation voltage	VsatVL	0.2	0.33	0.45	V	Iret = 0.1 A	3
OP Amp	Input current	Iinop	—	—	±500	nA		39, 41
	Input offset voltage	Vosop	—	—	(±7)	mV		1
	Common mode input voltage range	Vcmop	0	—	Vps - 0.2	V		
	Output high voltage	Vohop	Vps - 1.3	—	—	V	Iout = 1.0 mA	40
	Output low voltage	Volop	—	—	1.1	V	Iout = 1.0 mA	
Comparator	Input sensitivity	Vmin2	±9	0	—	mV		2, 3, 36
	Output low voltage	Volcp	—	—	0.4	V	I _o = 1 mA	36
	Output high voltage	Vohcp	V _{ss} - 1.8	—	V _{ss}	V	I _o = 1 mA	
Vref1	Output voltage	Vref1	—	4.0	±3%	V	I _o = 20 mA	37
	Output resistance	Ro1	—	—	5.0	Ω	I _o = 20 mA	
Power monitor	Threshold voltage	Vth3	-2%	1.39	+3%	V	V _{ss} = 5 V	44
	Hysteresis	Vhyspm1	25	40	55	mV	V _{ss} = 5 V	
	Threshold voltage	Vth4	-2%	1.38	+3%	V	V _{ss} = 4 V	21
	Hysteresis	Vhyspm2	25	40	55	mV	V _{ss} = 4 V	

Electrical Characteristics (Ta = 25°C, Vps = 12 V, Vss = 5 V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note	
POR	Output low voltage	V _{OL2}	—	—	0.4	V	I _o = 1 mA	29		
		V _{OL3}	—	—	0.4	V	I _o = 1 mA V _{SS} = Vps = 1.0 V			
	Output leak current	I _{cer5}	—	—	±10	μA	Vpor = 7 V			
	Threshold voltage	V _{th5}	—	1.4	±5%	V				22
	Charge current	I _{CH3}	—	6	±25%	μA				
	Discharge current	I _{DIS3}	40	—	—	mA				
OTSD	Operating temperature	Tsd	125	150	—	°C			1	
	Hysteresis	Thys	—	25	—	°C			1	

- Notes: 1. Design guide only.
 2. Variations of threshold voltage Vth3 and Vth4 depending on the power supply V_{SS} are shown in figure 4.

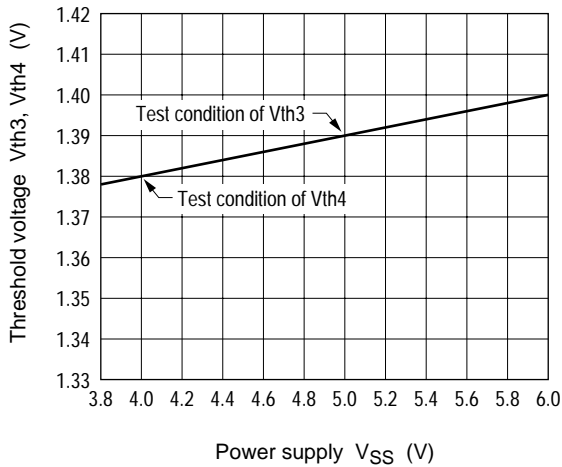
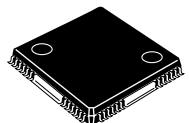
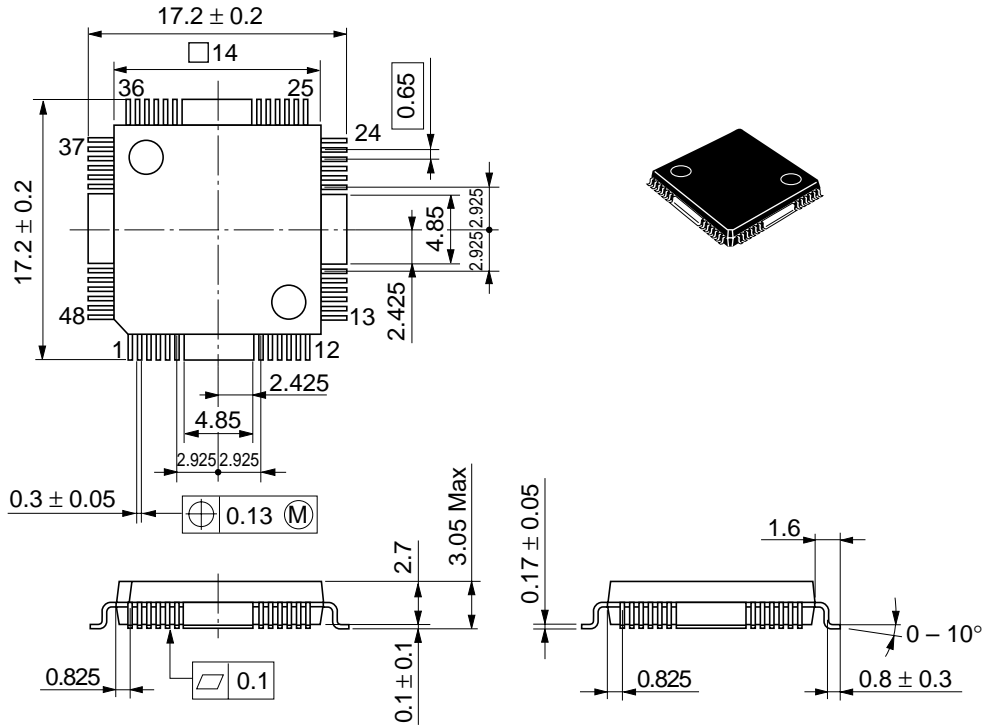


Figure 4

Package Dimensions

Unit: mm



Hitachi code	FP-48T
EIAJ code	—
JEDEC code	—

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